CS4223 Assignment 2

# Introduction

**Goal**: Simulate uniprocessor cache and multiprocessor with MSI and MESI cache coherence protocols.

**Assumptions made:**

1. When C1 does a BusRdX and C2 in a M state needs to flush, C1 gets the data after 10 cycles.
2. Each cache only has 1 pending instruction in the Bus
3. Cache hit includes cases where the cache block was found but a bus transaction still needs to be generated

# Implementation

//what the processor, cache, bus, etc. classes contain