CS4223 Assignment 2

# Introduction

**Goal**: Simulate uniprocessor and multiprocessor caches with MSI and MESI cache coherence protocols.

**Simulation Environment:**

1. Java Programming Language, Version 1.8
2. Eclipse IDE

**Assumptions made:**

1. A cache waiting for a flush gets the data only after 10 cycles
2. Each cache can only have 1 pending instruction in the Bus Request Queue
3. Cache hit includes cases where the cache block was found but a bus transaction still needs to be generated

# Implementation

//some stuff about the basic classes

* 1. Design

//about classes, flowcharts, how we calculate the cycles, bus traffic, etc.

## Results

1. What is the impact of cache size? Vary cache size between 1KB and 32KB.
2. 2. What is the impact of associativity? Vary associativity as 1, 2, 4
3. 3. What is the impact of the number of processors? Vary number of processors as 1, 2, 4, and 8
4. 4. What is the impact of block size? Vary block size between 8 byte and 128 byte
5. Data cache miss rate for each processor
6. Amount of Data traffic in bytes on the bus
7. Execution cycles per processor

//results for various files and various sizes of cache, no.processors, etc.

# Conclusion

//challenges and limitations faced

//conclude